CLAIMS

What is claimed is:

1. A method for utilizing fast analysis information during detailed analysis of a circuit design, comprising:

electronically analyzing one or more design blocks of the circuit design to determine fast analysis results based upon one or more assumptions of ported signal nets of each one of the design blocks;

determining whether hierarchical signal net connectivity of block instances of the design blocks matches the assumptions;

if the hierarchical signal net connectivity matches the assumptions, utilizing the fast analysis results to generate detailed analysis results; and

if the hierarchical signal net connectivity does not match the assumptions, electronically analyzing the one or more blocks to generate detailed analysis results.

2. The method of claim 1, the fast analysis results and detailed analysis results comprising FET leakage current.

3. The method of claim 1, wherein the assumptions specify that the ported signal nets do not connect to power nets.

4. The method of claim 1, wherein the assumptions specify that a ported signal net connected to a first FET within a design block also connects to a signal net connected to a second FET external to the design block, wherein the second FET is of the opposite type to the first FET.

5. The method of claim 1, further comprising generating assumption information defining which assumptions were utilized in determining the fast analysis results.

6. The method of claim 1, further comprising reading instantiation characteristics to determine the block instances.

7. A system for utilizing fast analysis information during detailed analysis of a circuit design, comprising:

a fast analysis tool for electronically analyzing one or more design blocks of the circuit design to determine fast analysis results based upon assumptions of ported signal nets of each one of the design blocks; and

a detailed analysis tool for determining whether hierarchical signal net connectivity of block instances of the design blocks matches the assumptions, the detailed analysis tool utilizing the fast analysis results to generate detailed analysis results when the hierarchical connectivity matches the assumptions and electronically analyzing instances of the one or more blocks to generate detailed analysis results when the hierarchical connectivity does not match the assumptions.

8. The system of claim 7, the fast analysis results and detailed analysis results comprising FET leakage current.

9. The system of claim 7, the assumptions specifying that the ported signal nets do not connect to power nets.

10. The system of claim 7, the assumptions specifying that a ported signal net connected to a first FET within a design block also connects to a signal net connected to a second FET external to the design block, wherein the second FET is of the opposite type to the first FET.

11. The system of claim 7, the fast analysis tool generating assumption information defining which assumptions were utilized in determining the fast analysis results.

12. The system of claim 7, the detailed analysis tool reading instantiation characteristics to determine the block instances.

13. The system of claim 7, further comprising a database for storing the fast analysis results for access by the detailed analysis tool.

14. The system of claim 13, the database storing the assumptions.

15. The system of claim 14, the database storing the detailed analysis results.

16. A system for utilizing fast analysis information during detailed analysis of a circuit design, comprising:

means for electronically analyzing one or more design blocks of the circuit design to determine fast analysis results based upon assumptions of ported signal nets of each one of the design blocks;

means for determining whether hierarchical signal net connectivity of block instances of the design blocks matches the assumptions;

means for utilizing the fast analysis results to generate detailed analysis results when the hierarchical signal net connectivity matches the assumptions; and

means for electronically analyzing the one or more blocks to generate detailed analysis results when the hierarchical signal net connectivity does not match the assumptions.

17. A software product comprising instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for utilizing fast analysis information during detailed analysis of a circuit design, comprising:

instructions for electronically analyzing one or more design blocks of the circuit design to determine fast analysis results based upon assumptions of ported signal nets of each one of the design blocks;

instructions for determining whether hierarchical signal net connectivity of block instances of the design blocks matches the assumptions;

instructions for utilizing the fast analysis results to generate detailed analysis results when the hierarchical signal net connectivity matches the assumptions; and

instructions for electronically analyzing the one or more blocks to generate detailed analysis results when the hierarchical signal net connectivity does not match the assumptions.

18. The software product of claim 17, wherein the assumptions specify that (a) the ported signal nets do not connect to power nets and (b) a ported signal net connected to a first FET within a design block also connects to a signal net connected to a second FET external to the design block, wherein the second FET is of the opposite type to the first FET.

19. The software product of claim 17, further comprising instructions for generating assumption information defining which assumptions were utilized in determining the fast analysis results.

20. The software product of claim 17, further comprising instructions for reading instantiation characteristics to determine the block instances.